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| INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i> | | | | Application Number | |
| | | | | Filing Date | J104D U.S. 02/28/01 |
| | | | | First Named Inventor | Michael J. Rendon |
| | | | | Group Art Unit | |
| | | | | Examiner Name | |
| Sheet | 1 | of | 2 | Attorney Docket Number | SC11814TP |

U. S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

Examiner Signature _____ Date Considered 6/14/02

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation, if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Unique citation designation number. ² See Kinds of U.S. Patent Documents. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English Language Translation is attached.

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| OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS | | | | | |
|--|-----------------------|---|--|--|----------------|
| Examiner Initials* | Cite No. ¹ | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | | | T ² |
| D | AC | Cheolmin Park et al., "50nm SOI CMOS Transistors with Ultra Shallow Junction using Laser Annealing and Pre-Amorphization Implantation", | | | |
| D | AD | Jung-Ho Lee et al., "Laser Thermal Annealed SSR well Prior to Epi-channel Growth (LASPE) for 70 nm nFETs", 2000 IEEE, IEDM 00-441, pgs. 18.4.1 – 18.4.4. | | | |
| D | AE | Ken-ichi Goto et al., "Ultra-Low Contact Resistance for Deca-nm MOSFETs by Laser Annealing", 1999 IEEE, IEDM-931-IEDM-933, pgs. 20.7.1 – 20.7.3. | | | |
| D | AF | Somit Talwar et al., "Ultra-Shallow, Abrupt, and Highly-Activated Junctions by Low-Energy Ion Implantation and Laser Annealing", 1999 IEEE, pgs. 1171-1174. | | | |
| D | AG | A. Sato et al., "Determination of Solid Solubility Limit of In and Sb in Si using Bonded Silicon-On-Insulator (SOI) Substrate, Proc. IEEE 1995 Int. Conference on Microelectronic Test Structures, Vol. 8, March 1995, pgs. 259-260. | | | |
| D | AH | Bin Yu et al., "70nm MOSFET with Ultra-Shallow, Abrupt, and Super-Doped S/D Extension Implemented by Laser Thermal Process (LTP)", 1999 IEEE, IEDM 99-509 – 99-512, pgs. 20.4.1 – 20.4.4. | | | |
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